Flip Chip Technologies

Course Leader: Shengmin Wen – HaiSemi Inc

Course Objective:
This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various type of wafer bumping technologies, substrate design and selection, underfill selection, Co-design and modeling, and reliability evaluation.

Two major assembly technologies, related equipment, materials, design rules, and design practices are covered in detail. Plenty of examples are presented to show the versatile flip-chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form interconnection such as wire bond/flip chip mixed integration. Major forms of flip chip assembly packages are discussed, such as the BGA packages, CSP packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages that uses Si or organic interposers, together with actual industrial leading application cases. In-depth discussions include chip package interaction (CPI), package warpage control, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, and Si die floor plan optimization, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their projects.

Various bumping technologies that are used in today's flip chip assembly are also briefly introduced, i.e., lead-free solder bumping and highly customized Cu-Pillar bumping. The course will also cover various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc.

Course Outline:

1. Introduction to Flip-Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Flip Chip Substrate Technologies,
5. Underfill, Package Warpage Control, and Yield Examples
6. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
7. Flip Chip Si Package Co-Design and Design Examples (BOT, BOP, AI type)
8. Flip Chip New Trends: Wafer Level CSP, Waver Lever Fan-Out, and Panel Level Packaging
9. Bumping Process, Rules, and introduction
10. Flip Chip Under-Bump Metal and Intermetallic
11. Review and Package Selection Exercise

Who Should Attend:
The goal of this course is to provide the students with fundamentals of flip chip packaging technology, to prepare the students with a list of options to apply to their particular flip chip assembly projects, and to achieve a reliable and cost-effective solution. Students are encouraged to bring packaging topics and technical questions from their past, present and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth

understanding of the flip chip assembly technologies, and are ready to meet their real-world packaging challenges.

BIO:

Dr. Shengmin Wen has more than 20 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume production business management. Recent years, he focuses on Si and package co-design that uses the most advanced flip chip integration methods, in particular organic RDL for 2.5D and 3D chiplet based integration, in addition to development of panel-based packaging that uses chip last flip chip methodologies. He has extensive and unique experiences in flip chip assembly technologies that use fine pitch Cu Pillar bump with both mass reflow and thermal compression processes. He is an expert in package warpage control, substrate technologies, advanced fine pitch flip chip assembly process, and reliability assessment. He currently works for SiMa Technologies, an Edge AI MLSoC, as Sr Director of packaging engineering, and he previously worked for JCET as VP and GM of design service BU, Synaptics Inc as the principal packaging architect, and Amkor Technology as director of 3D PoP and CSP Product Business Group.

Dr. Wen received his Ph.D. from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science-based fatigue theory. Dr. Wen has been actively participating and contributing to industry technical conferences to learn, to share, and to contribute.